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Serial Links Speed Serial Links  
Design Trends

# High Speed Serial Links Speed Serial Links Design Trends

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***SERDES Clocking and Equalization  
for High-Speed Serial Links, Jack  
Kenney*** Transcript: <https://resourcecenter.sscs.ieee.org/education/confedu-ci...>

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Slides: ...

***High Speed Serial Links by Dr. G.S.Javed (Founder, King Consultants - Education)*** In **high-speed** communication applications, a large amount of data may have to be communicated from one chip to another.

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*high speed i/o's*

***High Speed Serial Link Overview |  
Dr G S Javed*** A quick overview of the  
HSL !

***Why Every Car Needs These High-  
Speed Serial Links*** See why Gigabit  
Multimedia **Serial Link** (GMSL) SerDes

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technology provides the bandwidth needed to transport a burgeoning ...

## ***High Speed Serial Link 20 Gbps by Dr G S Javed (Founder, King Consultants Education) | IEEE CAS***

Topics and Timings are given below: This webinar is aimed at students who are interested in electronic circuit design

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## ***CTLE (Continuous Time Linear Equalizer) : HIGH SPEED SERDES***

This video discusses about CTLE; continuous time linear equalizer circuit.

## ***AWARE S1.EE: High-Speed Energy-Efficient Serial Links Serial data***

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**links** are nowadays employed almost everywhere. Within a traditional computer system, we can find a variety of **links** ...

***Addressing the Challenges of Serial Link Design and Analysis -- Cadence Design Systems High-speed serial interfaces present some of the biggest***

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challenges in board design today.  
Getting signal integrity right on your ...

## ***Interlaken IP : Ultra Scalable, High Speed, Serial Link-Based Chip-to- Chip Interface*** Open Silicon

Interlaken IP : Ultra Scalable, High  
Speed, Serial Link-Based Chip-to-Chip  
Interface

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From IP SoC India 2017 ...

***Serial Link Analysis*** This video focuses on **high speed serial link** analysis.

***HIGH SPEED SERDES  
(INTRODUCTION)*** This video discusses about **High speed SERDES. Serial** communication interface. Connectivity

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IP. It discusses at a very basic ...

**PCI Express Physical Layer** PCI Express Physical Layer An overview of PCI Express Physical Layer Technology - Part 1: Electrical by John Gulbrandsen, ...

**VLSIx 2016: Clock Recovery Architectures** Pavan Hanomlu

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Transcript: <https://resourcecenter.sscs.ieee.org/education/confedu-vl...> Slides: ...

***Phase Locked Loop Tutorial | PLL Basics*** Phase locked loops are used in many radio frequency of RF systems. Phase locked loops are used in radios, as FM detectors as ...

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**ESD (Part - 1)** I/O ESD & LATCHUP go together. I will cover all these in multiple videos. This is part 1.

**SERDES 1 Overview** This set of videos address SERDES or Serialize De-Serialize circuits like PCI Express, SATA, XAUI, etc. This is not a complete ...

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**SerDes Basics** This video describes the basics of Serdes serializer/deserializer technology and its benefits in the system.

## **Get Started AMBA® 3 AHB-Lite HD**

The AMBA 3 AHB-Lite interface specification enables highly efficient interconnect between simple peripherals

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in a subsystem ...

**SSCS CICCedu 2019 - A 56Gbps  
PAM4 ADC-Based Wireline  
Transceiver - Presented by Yohan  
Frans** Abstract: The emergence of PAM4  
electrical has caused wider adoption of  
ADC-based transceiver. This talk shows  
an example of ...

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**lecture32 - Decision feedback  
equalizers - elimination of noise  
enhancement**

Video Lecture Series by  
IIT Professors ( Not Available in NPTEL)  
VLSI Broadband Communication Circuits  
By Prof. Nagendra ...

**Signal Integrity Analysis of Serial  
Data Channels** Cadence Allegro Sigrity

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**Serial Link** Analysis is a full featured serial analysis solution that includes model extraction, topology ...

***ECE 623 Lecture on CDRs by Dr. Amr Elshazly*** On Sunday 21st of December 2014, Dr. Amr Elshazly of Intel gave a lecture on CDRs in the Integrated Circuits Laboratory ICL at ...

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**Energy-Efficient High Speed Serial  
Link Receiver** Energy-Efficient **High  
Speed Serial Link** Receiver □□□□□□□□.

**Efficient Test Methodologies for  
High Speed Serial Links Lecture  
Notes in Electrical Engineering**

**NIWeek2015: High Speed Serial**

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**Functional Test** For more information, visit <http://bit.ly/sdiniweek> This videos is a test of a **high-speed** communications DAC using the JESD 204B ...

***High Speed Serial Links - PHY Discussion | Terminus Circuits***

***Impact of High Speed Serial Links***

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### ***(HSS) in Embedded Computing***

"Impact of **High Speed Serial Links**  
(HSS) in Embedded Computing" Patrick  
Mechin, TechwaY.

***glscopeclient demo 2: High-speed  
serial*** Eye patterns, clock recovery,  
8B/10B decode, FFTs, and more!

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intermediate accounting 14th edition  
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sx100 owners manual

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